signal is contained in the linear composite signal that is produced by the adder 32S. In FIG. 22, the short codes SC_{S2}, SC_{S3} and SC_{S4} to be set in the correlators $32C_{12}$, $32C_{13}$ and $32C_{14}$ need not always be short codes of other user but may be those orthogonal to the short code SC_S, and orthogonal to one another as previously in the FIG. 9 embodiment. The weighting factors w_1 to w_4 in such a case can be determined by the same operation as described previously with reference to FIG. 9.

In the receivers described above in respect of FIGS. 6, 13 and 16, one delay circuit 36 may be inserted between the hybrid circuit 31 and the despreading part 32_1 corresponding to the direct path as depicted in FIG. 18 instead of inserting the two delay circuits 36_S and 36_L of each multipath separating part 30 (30_1, 30_2) between the short and long code generators 33_S and 33_L and the multipliers $32A_2$ and $32B_2$, respectively. Also in FIG. 17, the delay circuit 36 may be provided between the hybrid circuit 31H and the despreading part 32_1. In the receivers of the embodiments shown in FIGS. 6, 13, 15, 16 and 17, the multipath separating parts 30, 30_1 and 30_2 have been described on the assumption that the received wave is based on a two-wave model. In the cases of a three-wave model, a four-wave model and so forth, despreading branch paths corresponding to the number of delayed paths to be taken into account are added and despreading is carried out using short and long codes delayed by delay circuits of delay times corresponding to the respective delayed paths. For multipath components further added by the above operation, it is necessary only to add arrangements corresponding to the paths in the diversity detector 43 (FIG. 10A, 10B or 10C) to permit diversity detection of the added multipath components.

As described above, the receiver of the present invention permits diversity type detection with improved SN ratio through maximum utilization of the energies of multipath components. As a result, the bit error rate can be improved. By using interference cancelers as required, signal components of other users in the same cell can also be canceled—this further improves the transmission characteristic. Additionally, the receiver can also be designed so that the spectral bandwidth of the transmission wave remains unchanged even if the transmission rate is changed.

FIG. 23 shows computer simulation results which prove the effectiveness of the present invention. The spreading ratio was 16, the number of users was eight and the reception timing of the respective users was assumed to be synchronized. The modulation system used was a 10 Kb/s BPSK modulation system and codes of an auto-correlation below 0.25 were used as spreading codes. The propagation path model used was a two-path Rayleigh fading model and the delay time difference was T_C. The average En/No was 20 dB and the maximum Doppler frequency 80 Hz. In FIG. 23, N=1 shows the prior art and the average error rate is improved by the present invention which sets N to a value greater than 1. It is seen from FIG. 23 that the value N may preferably be 2, 3, 4 or so and that the improvement rate approaches saturation as the value N is further increased.

As described above, the present invention offers a spread spectrum transmitter and receiver which an excellent transmission characteristic over multipath propagation. Moreover, the channel capacity of the communication system can be significantly increased since interference components can effectively be canceled. The present invention is of great utility when employed in radio systems in which a large number of users share the same carrier frequency.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of the present invention.

What is claimed is:

1. A spread spectrum receiver employing composite spreading codes, comprising:
   - a receiving part for receiving a transmitted signal spectrum-spread by short and long codes to obtain a spread baseband received signal;
   - clock signal generating means for generating a first clock signal of a predetermined first clock period and a second clock signal of a second clock period N times longer than said first clock period, said N being larger than 1 but smaller than 8 and said second clock period being set longer than a predetermined delay time of a propagation path;
   - a short code generating means for repeatedly generating at least one short code of a chip period of the same length as that of said first clock period and of a first repetition period in synchronization with said first clock signal for each chip, said first repetition period of said short code being set equal to a symbol period;
   - a long code generating means for repeatedly generating a long code of a chip period longer than the chip period of said short code and of a second repetition period longer than said predetermined delay time of a propagation path and said first repetition period in synchronization with said second clock signal for each chip, the number of chips of said long code being greater than that of said short code;
   - a multipath separating part including a predetermined number of despreading parts each provided corresponding to one of a plurality of multipath components including a direct path component and at least one delayed path component, for despreading said spread baseband received signal from said receiving part by a pair of the short code and the long code in synchronization with said first and second clock signals, respectively at timing corresponding to an individual multipath and for outputting a despread signal corresponding to one of said plurality of multipath components; and
   - a diversity type detecting part for diversity-detecting despread signals from said predetermined number of despreading parts to detect a digital signal.

2. The receiver of claim 1, wherein said multipath separating part includes a delay circuit whereby a time difference corresponding to the delay time of a path delayed behind said direct path is set between timings for the despreading of said spread baseband received signal by said pair of short and long codes in said predetermined number of despreading parts.

3. The receiver of claim 2, wherein said predetermined number of despreading parts each include a multiplier for multiplying said spread baseband received signal by said pair of short and long codes.

4. The receiver of claim 3, wherein said delay circuit is provided to introduce said time difference in said pair of short and long codes which is applied to said multiplier of said despreading part corresponding to said delayed path.

5. The receiver of claim 3, wherein said delay circuit is provided to introduce said time difference in said spread baseband received signal which is applied to said multiplier of said despreading part corresponding to said direct path.

6. The receiver of claim 4 or 5, wherein said multipath separating part includes an exclusive-OR circuit for providing the exclusive OR of said short and long codes from said short and long code generating means as said pair of short and long codes.

7. The receiver of claim 2, wherein said multipath separating part includes a short code setting part for holding said